IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor formed between, and without including a portion of, said first trench isolation structure and said first impurity region, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer ~~defined in said first trench isolation region~~, said second impurity region being connected to a drain electrode of said first MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region of said second conductivity type provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises a buried impurity region of said second conductivity type provided directly below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer.

Claim 2 (Previously Presented): The semiconductor device according to claim 1, further comprising

a second trench isolation structure having a portion not connected to said first trench isolation structure and separated by a certain distance from said first trench isolation structure, said second trench isolation structure being provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said first impurity region, and said first trench isolation structure together defining said first trench isolation region in said RESURF isolation region.

Claim 3 (Currently Amended): [[The]] A semiconductor device ~~according to claim 1~~, comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer, said second impurity region being connected to a drain electrode of said first MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region of said second conductivity type provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises a buried impurity region of said second conductivity type provided directly below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

Claim 4 (Original): The semiconductor device according to claim 3,

wherein openings between adjacent ones of said plurality of conductive films are filled with said plurality of first insulating films.

Claim 5 (Currently Amended): [[The]] A semiconductor device ~~according to claim 2~~, comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with

said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer, said second impurity region being connected to a drain electrode of said first MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region of said second conductivity type provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises

a buried impurity region of said second conductivity type provided directly below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer, and

a second trench isolation structure having a portion not connected to said first trench isolation structure and separated by a certain distance from said first trench isolation structure, said second trench isolation structure being provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said

first impurity region, and said first trench isolation structure together defining said first trench isolation region in said RESURF isolation region,

wherein said first and second trench isolation structures each comprise an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

Claim 6 (Previously Presented): The semiconductor device according to claim 1, wherein said first trench isolation structure reaches said semiconductor substrate, and wherein an end portion of said first trench isolation structure reaches a depth shallower than the greatest depth of said buried impurity region.

Claim 7 (Currently Amended): [[The]] A semiconductor device ~~according to claim 1~~, comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a second conductivity type provided on said semiconductor substrate;

a first impurity region of said first conductivity type provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region;

a first trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region in said RESURF isolation region;

a semiconductor element provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor, comprising

a second impurity region of said second conductivity type provided in said upper surface of said semiconductor layer, said second impurity region being connected to a drain electrode of said first MOS transistor,

a third impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region of said second conductivity type provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises a buried impurity region of said second conductivity type provided directly below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer,

wherein said first trench isolation structure comprises an in-line portion which extends from said first impurity region towards said second impurity region, said in-line portion including

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of spaced-apart insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer, and

wherein said semiconductor device further comprises a fourth impurity region provided in said upper surface of said semiconductor layer defined in said RESURF isolation region, surrounding each one of said plurality of insulating films while filling openings between adjacent ones of said plurality of insulating films.

Claim 8 (Original): The semiconductor device according to claim 7,

wherein said fourth impurity region is depleted in its entirety when a PN junction between said fourth impurity region and said semiconductor layer is subjected to application of a reverse voltage.

Claim 9 (Original): The semiconductor device according to claim 1, further comprising

a second trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure and said first impurity region together defining a second trench isolation region in said RESURF isolation region, and

a second MOS transistor, comprising

a fourth impurity region of said second conductivity type provided in said upper surface of said semiconductor layer defined in said second trench isolation region, said fourth impurity region being connected to a drain electrode of said second MOS transistor,

a fifth impurity region of said first conductivity type provided in said upper surface of said semiconductor layer defined between said first and fourth impurity regions, and

a second source region of said second conductivity type provided in an upper surface of said fifth impurity region.

Claim 10 (Original): The semiconductor device according to claim 1, comprising

an interconnect line provided over said first trench isolation structure to be electrically connected to said drain electrode, and

a field plate held between said first trench isolation structure and said interconnect line,

wherein said field plate is a floating electrode, an electrode which is electrically connected to said semiconductor layer defined in said first trench isolation region, or an electrode which is electrically connected to said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region.

Claim 11 (Original): The semiconductor device according to claim 3, further comprising

a second insulating film provided on said semiconductor layer defined between said first impurity region and said buried impurity region, and

a plurality of field plates provided on said second insulating film,

wherein said plurality of conductive films are exposed from said upper surface of said semiconductor layer, and

wherein said plurality of field plates are respectively connected to said plurality of conductive films.

Claims 12-15 (Canceled).